UGC Major Research Project

Project Report on

Study of Quantum Dot Cellular Automata for designing circuits and implementing them for high speed and low power fault tolerant computing

File No: 41-631/2012(SR);

Date: 01/07/2012

2012-2015

Submitted by

Principal Investigator

Dr. Debashis De

Associate Professor

Computer Science & Engineering Department

West Bengal University of Technology

BF-142, Sector-I, Salt Lake City, Kolkata-700064, India

2017

Contents

To
G. S. Aulakh
Under Secretary
University Grants Commission
Bahadur Shah Zafar Marg
New Delhi – 110 002

Subject: Utilization Certificate, Final Statement of Expenditure and Project Completion Report of UGC Major Research Project No: 41-631/2012(SR); 01/07/2012

Dear Sir,

In response to your letter No: 41-631/2012(SR) dated 9 March 2017 I am submitting the Utilization Certificate, Final Statement of Expenditure and Project Completion Report of UGC Major Research Project No: 41-631/2012(SR); 01/07/2012 entitled "Study of Quantum Dot Cellular Automata for designing circuits and implementing them for high speed and low power fault tolerant computing".

Thanking you.

With Regards

(Debashis De)
Principal Investigator
Associate Professor
Computer Science & Engineering Department
West Bengal University of Technology
BF-142, Sector-I, Salt Lake City, Kolkata-700064, India

ANNEX: I

Financial Assistance provided/ Expenditure incurred:

Sl. No.	Items	Total Amount Sanctioned	Amount Approved in 1st Installment	Amount Approved in 2nd Installment (NOT RECEIVED)	Expenditure Incurred
1	Books & Journal	Rs. 70,000/-	Rs. 70,000/-		56,719/-
2	Equipments	Rs. 6,00,000/-	Rs. 6,00,000/-		5,99,959/-
3	Honorarium		nil		NA
4	Contingency	Rs. 80,000/-	Rs. 40,000/-		48,952/-
5	Travel/fieldwork	Rs. 75,000/-	Rs. 37,500/-		22,937/-
6	Chemicals & Glassware	Nil	Nil		
6	Hiring Services	Nil	Nil		
7	Overhead	Rs. 60,800/-	Rs. 60,800/-		60,800/-
8	Any other items (please specify)				
9	Honorarium to Principal Investigator				
10	Staff (date of appointment) (from Dec. 2012 to Jan. 2014) (Please give details of staff appointed in the prescribed format)	Rs. 5,28,000/-	Rs. 2,64,000/-		3,67,097/-
	Total	Rs. 14,13,800/-	Rs. 10,72,300/-		Rs. 11,56,464/-

It is Certified that the 1st installment grant of Rs. 10, 72,300/- (Rupees Ten Lakh Seventy Two Thousand and Three Hundred only) received from the University Grants Commission under the scheme of support for Major Research Project entitled: “Study of Quantum Dot Cellular Automata for designing circuits and implementing them for high speed and low power fault tolerant computing”, vide UGC Letter No. F.41-631, Dated 01/07/2012.The total sanction amount is Rs.14,138,000/-. Out of which a sum of Rs. 11, 56,464/- (Rupees Eleven Lakh Fifty Six Thousand Four Hundred and Sixty Four and only) has been utilized for the purpose of which it was sanctioned in accordance with the terms and condition laid down by the University Grant Commission.

PRINCIPAL INVESTIGATOR **REGISTRAR**

(SIGNATURES WITH SEAL) **(SIGNATURES WITH SEAL)**

ANNEX: II

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002

Utilization certificate

Certified that the 1st installment grant of Rs. 10, 72,300/- (Rupees Ten Lakh Seventy Two Thousand and Three Hundred only) received from the University Grants Commission under the scheme of support for Major Research Project entitled: "Study of Quantum Dot Cellular Automata for designing circuits and implementing them for high speed and low power fault tolerant computing", vide UGC Letter No. F.41-631, Dated 01/07/2012.The total sanction amount is Rs.14,138,000/-. Out of which a sum of Rs. 11, 56,464/- (Rupees Eleven Lakh Fifty Six Thousand Four Hundred and Sixty Four and only) has been utilized for the purpose of which it was sanctioned in accordance with the terms and condition laid down by the University Grant Commission.

PRINCIPAL INVESTIGATOR	**REGISTRAR**	**FINANCE OFFICER**

ANNEX : V

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002
PROFORMA FOR SUBMISSION OF INFORMATION AT THE TIME OF SENDING THE FINAL REPORT OF THE WORK DONE ON THE PROJECT

1. TITLE OF THE PROJECT: STUDY OF QUANTUM DOT CELLULAR AUTOMATA FOR DESIGNING CIRCUITS AND IMPLEMENTING THEM FOR HIGH SPEED AND LOW POWER FAULT TOLERANT COMPUTING.

2. NAME AND ADDRESS OF THE PRINCIPAL INVESTIGATOR : DR. DEBASHIS DE, OFFICE: MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL (FORMERLY KNOWN AS WEST BENGAL UNIVERSITY OF TECHNOLOGY). BF142, SECTOR 1, SALT LAKE CITY, KOLKATA 700 009 RESIDENTIAL: 43, ANANDA MOHAN BOSE ROAD, DUM DUM, KOLKATA 700 009

3. NAME AND ADDRESS OF THE INSTITUTION: MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL (FORMERLY KNOWN AS WEST BENGAL UNIVERSITY OF TECHNOLOGY). BF142, SECTOR 1, SALT LAKE CITY, KOLKATA 700 009

4. UGC APPROVAL LETTER NO. AND DATE: NO: 41-631/2012(SR) DATE 16 JULY 2012

5. DATE OF IMPLEMENTATION: 01.07.2012

6. TENURE OF THE PROJECT: 01.07.2012 to 31.12.2015

7. TOTAL GRANT ALLOCATED: 14,13,800/-

8. TOTAL GRANT RECEIVED IN 1st INSTALMENT: 10,72,300/-

9. FINAL EXPENDITURE: 11, 56, 464/-

10. TITLE OF THE PROJECT: STUDY OF QUANTUM DOT CELLULAR AUTOMATA FOR DESIGNING CIRCUITS AND IMPLEMENTING THEM FOR HIGH SPEED AND LOW POWER FAULT TOLERANT COMPUTING.

11. OBJECTIVES OF THE PROJECT:

a. Combinational and sequential logic circuit design using reversible logic and tile structure of QCA.
b. Universal logic gate design and there implementation in different circuit.
c. Testable conservative logic circuit design.
d. Fault analysis and measurement of the defect tolerance of the logic circuits.
e. Analysis of the impact of scaling on defects that may arise in the manufacturing of QCA devices.

f. ALU and FPGA design using reversible logic.
g. Analysis of the temperature independent operation of QCA.
h. Power dissipation estimation and calculation of circuit costs.
i. Study of III-V, II-VI, IV-VI nano semiconducting materials for QCA application and subsequent suggestion for fabrication.

12. WHETHER OBJECTIVES WERE ACHIEVED

Yes, the objectives have been achieved. In this project we proposed various fault tolerant computational circuit design using QCA. Firstly we present a review work on various Reversible logic gates that have been designed in QCA paradigm. Different variations of the design done on basic reversible gates like Fredkin Gate, Toffoli Gate and Feynman Gate are studied. Also some of the modifications done on earlier gates as well as some new reversible gate that have been proposed in latter literature are highlighted. Next an optimized and efficient design of XOR and Decoders are implemented using QCA. The design of the decoders by repeated use of the XOR gate helps to reduce the cell count to a large extent. Finally the 4X16 decoder is utilized to design a decoder based PLA circuit. The PLA can be used to perform various logic operations; here a 2-bit adder has been designed. Then we design a QCA based cryptographic system. The proposed system provides two phases of security. With increasing number of bits, the sequence can be extended up to a large number of combinations. Finally a novel molecular QCA structure has been explored. A variation of hexaborate dianion is utilized as the central molecule. The simulation result of the proposed molecular QCA shows the charge quantization. We have also shown the redox reaction between the central dianion and the corner resonating molecules. The bistability of the proposed molecule is proved by the HOMO LUMO plot obtained after DFT calculation. Further the simulation has been performed in 300K which establishes the possibility of room temperature fabrication of molecular QCA structure.

Besides, the fault due to the missing cell, additional cell disposition and misplaced cell alignments of the QCA circuits have been analyzed and a possible solution have been proposed for fault free implementation of the QCA circuits. The stuck at fault analysis is also performed and set of test vectors have been proposed to identify the faults. Those fault analysis has been performed on QCA based circuits like SISO shift register, parity generator, parity checker, binary incrementer, flip-flops, etc. The power dissipation by the QCA circuits has been estimated which shows that the QCA circuits exhibits very low power dissipation and suitable for implementation of reversible circuits. For reversible QCA circuits, the circuit cost, i.e., quantum cost has been calculated and compared with traditional reversible circuits that yield cost effective design in QCA. To protect information from unauthorized access, cryptographic and steganographic architecture have been achieved and also shown how secure communication can be performed through those architectures.

13.

I. ACHIEVEMENTS FROM THE PROJECT:

a. Various fault tolerant non-reversible computational circuit like XOR gate, adder, comparator, multiplexer, demultiplexer, universal shift register, parity generator, parity checker, binary incrementer, flip-flops, decoders, PLA circuit etc design using QCA.
b. Various fault tolerant reversible computational circuit for Fredkin Gate, Toffoli Gate and Feynman Gate, BJN gate, Peres gate, RUG gate, QCA1 and QCA2 gate CQCA gate, multiplexer, demultiplexer, parity generator, parity checker, binary incrementer, code converters, etc design using QCA.

c. Various QCA based design of Nanocommunication architecture having components like router, multiplexer, demultiplexer, parity generator, parity checker in reversible as well as non reversible approach.
d. Cryptographic and sterganographic architecture in QCA.
e. Fault free implementation of QCA circuits through analyzing the missing cell, additional cell disposition and misplaced cell alignments based defects in QCA circuits
f. Low power QCA circuits to process information at very fast operating speed.
g. For reversible QCA circuits, the circuit cost, i.e., quantum cost has been calculated and compared with traditional reversible circuits that yield cost effective design in QCA.
h. To protect information from unauthorized access, cryptographic and steganographic architecture have been achieved and also shown how secure communication can be performed through those architectures.

II. AWARDS RECEIVED:

a. Best paper award for the paper entitled "Towards quantum dot and device implementation with InP–GaAs–InP nanostructure" in 3rd International Conference NANOCON-14), Pune, India, 2014.
b. Best paper award for the paper entitled "Arithmetic Overflows Detection Using Quantum-Dot Cellular Automata," in 3rd International Conference on Microelectronics, Circuits and Systems (MICRO-2016), Kolkata, West Bengal, India, 2016.
c. Second Best Paper award for the paper entitled "Quantum-Dot Cellular Automata Based Design of Reversible Controllable Inverter" in NanoBioCon-2016, Kolkata, West Bengal, India, 2016.
d. Best Poster Presentation award for the paper entitled "Fringe Print Authentication Using QCA Technology" in NanoBioCon-2016, Kolkata, West Bengal, India, 2016.
e. A. J. C. BOSE Memorial Award in IETE Journal of Research for the paper entitled "Reversible Binary to Grey and Grey to Binary Code Converter using QCA," IETE J. Res., vol. 61, no. 3, pp. 223-229, 2016.

14. SUMMARY OF THE FINDINGS

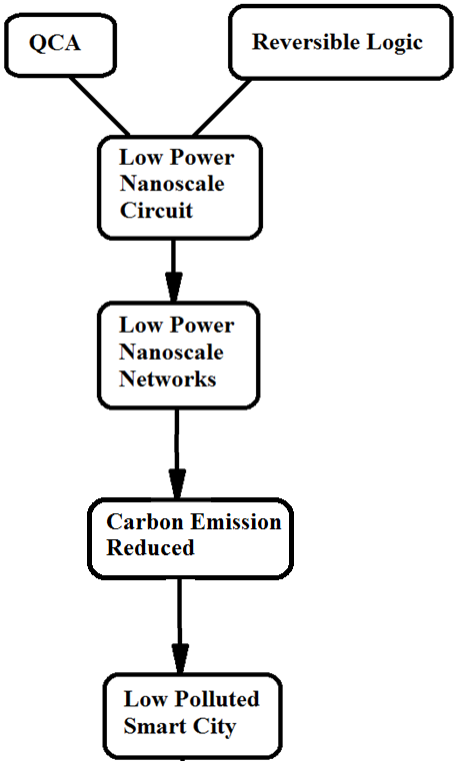
a. Low power nano-scale fault tolerant reversible and non-reversible computational circuits for XOR gate, adder, comparator, multiplexer, demultiplexer, universal shift register, parity generator, parity checker, binary incrementer, flip-flops, decoders, PLA circuit, Fredkin Gate, Toffoli Gate and Feynman Gate, BJN gate, Peres gate, RUG gate, QCA1 and QCA2 gate CQCA gate, code converters, etc.
b. Nanocommunication architecture in reversible as well as non reversible approach.
c. Cryptographic and sterganographic architecture in QCA.
d. It has been observed that QCA circuits exhibits high computational efficiency at very low temperatures and low computational efficiency at higher temperatures.
e. During fabrication the miss alignment of QCA cells has diverse effects on the circuit which may cause in generation of faulty outputs.
f. Low power dissipation by QCA circuits is suitable for implementation of reversible circuits.
g. QCA circuits have lower circuit cost, i.e., quantum cost that yield cost effective design than traditional circuits.
h. Power analysis attack can be prevent through QCA based cryptographic and steganographic architectures.

15. CONTRIBUTION TO THE SOCIETY

This Project introduced a new and efficient way of circuit designing. In the growing trend of Digital India and Smart Cities our project finds high contribution to the society. This is because in this project we have focused on two major challenges in electronic circuit designs i.e. power dissipation and speed of computation. In all the papers that have been published in this project our proposed designs have excelled in these two aspects, as shown in the comparative studies. Further we have put effort in designing bio-molecular based circuits which encourages the usage of renewable energies.

Therefore, the contributions to the society are summarized as follows:

a. Due to high device density of QCA circuit, nanoscale circuit can be achieved. It helps to reduce the device area and fabrication at nano-level.
b. Low power dissipation helps low power networks that are useful to build up low polluted smart city.
c. The environment will be healthy and the people will also be healthy.



16. WHETHER ANY PH.D. ENROLLED/PRODUCED OUT OF THE PROJECT: YES
    1. TAMOGHNA PURKAYASTHA
    2. KUNAL DAS
    3. JADAV CHANDRA DAS

17. NO. OF PUBLICATIONS OUT OF THE PROJECT
    Peer Reviewed Journals: 32
    International Conference: 12
    Book: 1
    Book Chapter:1

LIST OF PUBLICATIONS OUT OF THE PROJECT

SCI Indexed Journal:

1. Kunal Das, **Debashis De** and Mallika De "Realization of Semiconductor ternary Quantum dot Cellular Automata" IET Micro & Nano Letters, Volume 8, Issue 5, May 2013, p. 258 – 263, Online ISSN 1750-0443 Impact factor 1.06 (Thomson Reuters, Journal Citation Reports).
2. Purkayastha, Tamoghna, Tanay Chattopadhyay, and **Debashis De**. "Design of reversible logic circuits using quantum dot cellular automata-based system."Nanotechnology Reviews 4.5 (2015): 375-392. (Thomson Reuters Indexed)
3. Purkayastha, Tamoghna, **Debashis De**, and Kunal Das. "A novel pseudo random number generator based cryptographic architecture using quantum-dot cellular automata."Microprocessors and Microsystems 45 (2016): 32-44.(Thomson Reuters Indexed)
4. **Debashis De,** Tamoghna Purkayastha, and Tanay Chattopadhyay. "Design of QCA based Programmable Logic Array using decoder."Microelectronics Journal 55 (2016): 92-107.(Thomson Reuters Indexed)
5. Purkayastha, Tamoghna, **Debashis De**, and Tanay Chattopadhyay. "Universal shift register implementation using quantum dot cellular automata."Ain Shams Engineering Journal (2016).(Thomson Reuters Indexed)
6. Tamoghna Purkayastha, **Debashis De**, Kunal Das. "Towards quantum dot and device implementation with InP–GaAs–InP nanostructure."Nanomaterials and Energy 5.1 (2016): 20-27.(Thomson Reuters Indexed)
7. J. C. Das, and **Debashis De**, "Novel Low Power Reversible Binary Incrementer Design Using Quantum-Dot Cellular Automata," Microprocess. Microsyst., vol. 42, pp. 10-23, 2016. (Thomson Reuters Indexed)
8. J. C. Das, and **Debashis De**, "Operational Efficiency of Novel SISO Shift Register Under Thermal Randomness in Quantum-Dot Cellular Automata Design," Microsystem Technologies, vol. , pp. , 2016, doi: 10.1007/s00542-016- 3085-y. (Thomson Reuters Indexed)
9. J. C. Das, and **Debashis De**, "Quantum Dot-Cellular Automata Based Reversible Low Power Parity Generator and Parity Checker Design for Nanocommunication," Front. Inf. Technol. Electron. Eng., vol. 17, no. 3, pp. 224-236, Mar. 2016. (Thomson Reuters Indexed)
10. B. Debnath, J. C. Das and **Debashis De**, "Reversible Logic Based Image Steganography Using QCA for Secure Nanocommunication," IET Circuits Devices and Systems, 2016. doi:10.1049/iet-cds.2015.0245. (Thomson Reuters Indexed)
11. J. C. Das and **Debashis De**, "Reversible Comparator Design using Quantum Dot-Cellular Automata," IETE J. Res., vol. 62, no. 3, pp. 323-330, 2016. doi: 10.1080/03772063.2015.1088407. (Thomson Reuters Indexed)
12. J. C. Das and **Debashis De**, "Reversible Binary to Grey and Grey to Binary Code Converter using QCA," IETE J. Res., vol. 61, no. 3, pp. 223-229, May 2015. (Thomson Reuters Indexed)
13. J. C. Das and **Debashis De**, "Novel Low Power Reversible Encoder Design Using Quantum-Dot Cellular Automata," Nanoelectron. Optoelectron., vol. 11, no.4, pp. 450-458, 2016. (Thomson Reuters Indexed)
14. J. C. Das, and **Debashis De**, "User Authentication Based on Quantum-Dot Cellular Automata Using Reversible Logic for Secure Nanocommunication," Arab J Sci Eng, vol. 41, no. 3, pp. 773-784, Mar. 2016. (Thomson Reuters Indexed)
15. J. C. Das, and **Debashis De**, "Reversible Binary Subtractor Design Using Quantum Dot-Cellular Automata," Front. Inf. Technol. Electron. Eng., 2016. Doi:10.1631/FITEE.1600999. (Thomson Reuters Indexed)
16. J. C. Das, and **Debashis De**, "Optimized Multiplexer Design and Simulation using Quantum Dot-Cellular Automata," Indian Journal of Pure & Applied Physics, vol. 54, no. 12, pp. 802-811, Dec. 2016. (Thomson Reuters Indexed)
17. J. C. Das, and **Debashis De**, "Optimized Design of Reversible Gates in Quantum Dot-Cellular Automata: A Review", Rev. Theor. Sci., vol. 4, no. 3, pp. 279–286, 2016. (Thomson Reuters Indexed)
18. J. C. Das, T. Purkayastha, and **Debashis De**, "Reversible Nano-Router Using QCA for Nanocommunication," Nanomaterials and Energy, vol. 5, no. 1, pp. 28–42, Jan. 2016, doi: 10.1680/jnaen.15.00012. (Thomson Reuters Indexed)
19. J. C. Das, and **Debashis De**, "Shannon's Expansion Theorem Based Multiplexer Synthesis Using QCA," Nanomaterials and Energy, vol. 5, no. 1, pp. 53–60, Jan. 2016, doi: 10.1680/jnaen.15.00008. (Thomson Reuters Indexed)
20. B. Debnath, J. C. Das, and **Debashis De**, "Correlation and convolution for binary image filter using QCA," Nanomaterials and Energy, vol.5 no. 1, pp. 61–70, 2016, doi: 10.1680/jnaen.15.00010(Thomson Reuters Indexed)

21. J. C. Das, B. Debnath, and **Debashis De**, "Reversible Gate Based Cipher Text Using QCA for Nanocommunication," Nanomaterials and Energy, 2016 (Accepted) (Thomson Reuters Indexed)
22. J. C. Das, B. Debnath, and **Debashis De**, "Atbash Cipher Design for Secure Nanocommunication Using QCA," Nanomaterials and Energy, 2016 (Accepted). (Thomson Reuters Indexed)
23. Das, Kunal, **Debashis De**, and Mallika De. "Modified Ternary Karnaugh Map and Logic Synthesis in Ternary Quantum Dot Cellular Automata." *IETE Journal of Research* 62.6 (2016): 774-785. (Thomson Reuters Indexed)
24. A Dey, K Das, **Debashis De**, M De, S Das, Fan-out constraints in quantum dot cellular automata circuit design, Nanomaterials and Energy 5 (1), 43-52 (Thomson Reuters Indexed)

Peer-Reviewed International Journal:

25. Kunal Das, **Debashis De**, Mallika De, "Competent Universal Reversible Logic Gate Design for Quantum dot Cellular Automata", WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS. Issue 12, Volume 11, pp. 401-411, December 2012.
26. ArijitDey, Kunal Das, **Debashis De**, Mallika De, "Probabilistic Defect Analysis Model for Quantum dot Cellular Automata Design at Analytical Phase", International Journal of Computer Applications Published by Foundation of Computer Science, New York, USA.55(7):33-41, October 2012.
27. J. C. Das, and **Debashis De**, "Reversible Half-Adder Design Using Quantum Dot-Cellular Automata," Quantum Matter, Vol.5, No.4, pp. 476-491, 2016.
28. J. C. Das, and **Debashis De**, "Optimized Design of Flip-Flops Using Quantum-Dot Cellular Automata," Quantum Matter, vol.5, no.5, pp. 680-688, 2016.
29. Purkayastha, Tamoghna, Tanay Chattapadhaya, **Debashis De**. "Realization of data flow in QCA tile structure circuit by potential energy calculation."Procedia Materials Science 10 (2015): 353-360.
30. J. C. Das, B. Debnath, and **Debashis De**, "Image Steganography using Quantum dot Cellular Automata," Quantum Matter, vol. 4, no. 5, pp. 504-517, 2015.
31. T. Purkayastha1, J. C. Das, M. S. Habibullah, and **Debashis De**, "Quantum-Dot Cellular Automata Based Autonomous System for Future Nano-Communication Device," Quantum Matter, Vol.5, No.6, pp. 725–731, 2016.
32. J. C. Das, B. Debnath, and **Debashis De**, "Area Efficient Low Power Scan Flip-Flop Design Based on Quantum-Dot Cellular Automata," Adv. Ind. Eng. Manag., vol. 1 no. 1, pp. 157-164, 2016, doi: 10.7508/aiem.2016.01.030.

International Conferences:

1. Purkayastha, Tamoghna, Tanay Chattapadhaya, **Debashis De,** Biplab Das. "First principle study of molecular quantum dot cellular automata using mixed valence compounds."Devices, Circuits and Systems (ICDCS), 2016 3rd International Conference on. IEEE, 2016.

2. J. C. Das, B. Debnath, and **Debashis De**, "Arithmetic Overflows Detection Using Quantum-Dot Cellular Automata," 3rd International Conference on Microelectronics, Circuits and Systems, MAKAUT, West Bengal, Kolkata, India, pp. 404-409, 2016.

3. B. Debnath, J. C. Das, **Debashis De**, and T. Ghosh, "Image Masking Using Quantum-dot Cellular Automata," 3rd International Conference on Devices, Circuits and Systems, Karunya University, Tamilnadu, India, 2016. doi: 10.1109/ICDCSyst.2016.7570598.

4. J. C. Das, **Debashis De**, and T. Sadhu, "A Novel Low Power Nanoscale Reversible Decoder Using Quantum-dot Cellular Automata for Nanocommunication," 3rd International Conference on Devices, Circuits and Systems, Karunya University, Tamilnadu, India, 2016. doi: 10.1109/ICDCSyst.2016.7570597.

5. Das, Jadav Chandra, and **Debashis De**. "**Quantum Dot-Cellular Automata based cipher text design for nano-communication**." Radar, Communication and Computing (ICRCC), 2012 International Conference on. IEEE, 2012.

6. Pradhan, Nilanjana, and **Debashis De**. "**Spin Transfer Torque Driven Magnetic QCA Cells.**" Advanced Nanomaterials and Nanotechnology. Springer Berlin Heidelberg, 2013. 561-569.

7. **Das, Soumyadip, and Debashis De**. "**Nanocommunication using QCA: A data path selector cum router for efficient channel utilization.**" Radar, Communication and Computing (ICRCC), 2012 International Conference on. IEEE, 2012.

8. Pradhan, Nilanjana, Kunal Das, and **Debashis De**. "**Diverse clocking strategy in MQCA**." Recent Advances in Information Technology (RAIT), 2012 1st International Conference on. IEEE, 2012.

9. Roy, Pradipta, Debarati De,Swati Sinha**, Debashis De** "**Reversible OR Logic Gate Design Using DNA.**" Proceedings of Seventh International Conference on Bio-Inspired Computing: Theories and Applications (BIC-TA 2012). Springer India, 2013.

10. Kunal Das**, Debashis De**, Sayantan Ghatak, Mallika De "**Re-Programmable Logic Array for Logic Design and Its Reliability Analysis in QCA**" Accepted in National Conference ETCC2014 and will be published in Springer Lecture Notes in Electrical Engineering.

11. Dipannita Podder, Kunal Das, **Debashis De**, Mallika De "**Realization of Bi-quinary Coded Decimal Adder in Quantum dot Cellular Automata**" Accepted in National Conference ETCC2014 and will be published in Springer Lecture Notes in Electrical Engineering.

12. Arijit De, Kunal Das, **Debashis De**, Mallika De "**Online Testable Conservative Adder Design in Quantum dot Cellular Automata**" Accepted in National Conference ETCC2014 and will be published in Springer Lecture Notes in Electrical Engineering.

Book:

1. **"Quantum Dots and Quantum Cellular Automata: Recent Trends and Applications",** by **Debashis De**, Sitanshu Bhattacharaya and K. P. Ghatak (Department of Computer Science and Engineering, West Bengal University of Technology, Salt Lake City, Kolkata, India, and others), NOVA publishers.

Book Chapter:

1. Kunal Das, Arijit Dey , Dipannita Podder, Mallika De, **Debashis De**. Quantum Dot Cellular Automata: A Promising Paradigm Beyond Moore. In "Computational Intelligence in Digital and Network Designs and Applications" 2015 (pp. 295-323). Springer International Publishing.

_____ _____

(PRINCIPAL INVESTIGATOR) **(REGISTRAR/PRINCIPAL)**

ANNEX: IX

ज्ञान–विज्ञान विमुक्तये

PROFORMA FOR SUPPLYING THE INFORMATION IN RESPECT OF THE STAFF APPOINTED UNDER THE SCHEME OF MAJOR RESEARCH PROJECT UGC File No F. 41-631/2012(SR)(MRP) years 2012 COMMENCEMENT

TITLE OF THE PROJECT:

Study of Quantum Dot Cellular Automata for designing circuits and implementing them for high speed and low power fault tolerant computing

1.	Name Of the Principal Investigator:	Prof./Dr. Debashis De
2.	Name of the University/College	Department of Computer Science and Engineering, West Bengal University of Technology
3.	Name of the Research Personnel Appointed	Tamoghna Purkayastha
4.	Academic qualification	M.Tech in VLSI Design, B.Tech in Electronics and Communication Engineering
5.	Date of joining	06/01/2014
6.	Date of Birth of Research Personnel	18/11/1986
7.	Amount of HRA, if drawn	NIL
8.	Number of Candidate applied for the post	06

CERTIFICATE

THIS IS TO CERTIFY THAT ALL THE RULES AND REGULATIONS OF UGC MAJOR RESEARCH PROJECT OUTLINED IN THE GUIDELINES HAVE BEEN FOLLOWED. ANY LAPSE ON THE PART OF THE UNIVERSITY WILL LIABLE TO TERMINATE OF SAID UGC PROJECT.

PRINCIPALINVESTIGATOR **HEAD OF THE DEPT.** **REGISTRAR/PRINCIPAL**

PROFORMA FOR SUPPLYING THE INFORMATION IN RESPECT OF THE STAFF APPOINTED UNDER THE SCHEME OF MAJOR RESEARCH PROJECT UGC File No F. 41-631/2012(SR)(MRP) years 2012 COMMENCEMENT

TITLE OF THE PROJECT:

Study of Quantum Dot Cellular Automata for designing circuits and implementing them for high speed and low power fault tolerant computing

1.	**Name Of the Principal Investigator:**	**Prof./Dr. Debashis De**
2.	**Name of the University/College**	**Department of Computer Science and Engineering, West Bengal University of Technology**
3.	**Name of the Research Personnel Appointed**	**Soumyadip Das**
4.	**Academic qualification**	**M.Tech in VLSI Design, M. Sc. in Electronic Science**
5.	**Date of joining**	**18/12/2012**
6.	**Date of Birth of Research Personnel**	**19/09/1985**
7.	**Amount of HRA, if drawn**	**NIL**
8.	**Number of Candidate applied for the post**	**02**

CERTIFICATE

THIS IS TO CERTIFY THAT ALL THE RULES AND REGULATIONS OF UGC MAJOR RESEARCH PROJECT OUTLINED IN THE GUIDELINES HAVE BEEN FOLLOWED. ANY LAPSE ON THE PART OF THE UNIVERSITY WILL LIABLE TO TERMINATE OF SAID UGC PROJECT.

PRINCIPAL INVESTIGATOR **HEAD OF THE DEPTT.** **REGISTRAR/PRINCIPAL**

ANNEX: VI

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002

MAJOR RESEARCH PROJECT COPY OF THE SPECIMEN OF HOUSE RENT FOR POST-DOCTORAL FELLOW / PROJECT ASSOCIATE / PROJECT FELLOW

Certified that Shri/Dr.___NA is paying House Rent of Rs. _____NA_____ and is eligible to draw House Rent Allowances @ _____NA_____ as per University Rules.

_____
Registrar/Principal
(Signature with Seal)

Certified that **Shri**/Dr**.** **TAMOGHNA PURKAYASTHA**___is not staying independently and therefore is eligible to draw House Rent @ of **Rs. __4,200p.m. (30% of 14,000 pm for initial one year)** and **Rs. 4,800 p.m. (30% of 16,000 pm for final one year)** minimum admissible to a Lecturer as per University Rules.

_____
Registrar/Principal
(Signature with Seal)

Certified that Shri/Dr._____NA_____ has been provided accommodation in the Hostel. But he/she could not be provided with single seated flat type accommodation as recommended by the Commission, Hostel fee @ Rs._____NA_____ per month w.e.f. _____NA_____ is being charged from him/her.

_____
Registrar/Principal
(Signature with Seal)

HRA CALCULATION OF PRESENT PROJECT FELLOW

FOR THE YEAR 2014 and 2015

YEAR	FELLOWSHIP	HRA @ 30%	TOTAL HRA
Jan 2014 to Dec 2014 (Second Year)	Rs 14000 p.m	Rs 4200	Rs 49840
Jan 2015 to Dec 2015 (Third Year)	Rs 16000 p.m	Rs 4800	Rs 57600
			Rs 107440

Principal Investigator
(Signature with Seal)

Registrar/Principal
(Signature with Seal